Amendments to the Claims

Claim 1 **(Currently Amended)** A clock conversion apparatus for converting data synchronized with a first clock into data synchronized with a second clock, the clock conversion apparatus comprising:

a memory having a number of addresses that is less than a number of addresses required for storage of data corresponding to a predetermined period, and being able to execute a writing operation and a reading operation independently from each other using a clock for writing and a clock for reading, respectively;

a first counter circuit for counting the first clock, and generating write addresses of the memory so that the data corresponding to the predetermined period can be written into the memory over ~~using at least a portion of the addresses of the memory~~ a plurality of times; and

a second counter circuit for counting the second clock, and generating read addresses of the memory so that the data corresponding to the predetermined period, which have been written in the memory, can be read from the memory over ~~using at least the portion of the addresses of the memory~~ a plurality of times.

Claim 2 **(Currently Amended)** A clock conversion apparatus for converting data synchronized with a first clock into data synchronized with a second clock, the clock conversion apparatus comprising:

a memory having a number of addresses that is less than a number of addresses required for storage of data corresponding to a predetermined period, and being able to execute a writing operation and a reading operation independently from each other using a clock for writing and a clock for reading, respectively;

a first counter circuit for starting a count of the first clock on receipt of a writing start reference signal indicating a reference timing of starting data writing into the memory, and generating write addresses of the memory so that the data corresponding to the predetermined period can be written in the memory over ~~using at least a portion of the addresses of the memory~~ a plurality of times; and

a second counter circuit for starting a count of the second clock from a reading start reference signal indicating a reference timing of starting data reading from the memory, and

generating read addresses of the memory so that the data corresponding to the predetermined period, which have been written in the memory, can be read from the memory over ~~using at least the portion of the addresses of the memory~~ a plurality of times.

Claim 3 **(Currently Amended)** A clock conversion apparatus for converting data synchronized with a first clock into data synchronized with a second clock, the clock conversion apparatus comprising:

a memory having a number of addresses that is less than a number of addresses required for storage of data corresponding to a predetermined period, and being able to execute a writing operation and a reading operation independently from each other using a clock for writing and a clock for reading, respectively;

a first counter circuit for starting a count of the first clock on receipt of a writing start reference signal indicating a reference timing of starting data writing into the memory, and generating write addresses of the memory so that the data corresponding to the predetermined period can be written into the memory over ~~using at least a portion of the addresses of the memory~~ a plurality of times;

a second counter circuit for starting a count of the second clock from a reading start reference signal indicating a reference timing of starting data reading from the memory, and generating read addresses of the memory so that the data corresponding to the predetermined period, which have been written in the memory, can be read from the memory over ~~using at least the portion of the addresses of the memory~~ a plurality of times; and

a delay adjustment circuit operable to adjust a delay time, which delays the writing start reference signal to generate the reading start reference signal.

Claim 4 **(Currently Amended)** A clock conversion apparatus for converting data synchronized with a first clock into data synchronized with a second clock, the clock conversion apparatus comprising:

a memory having a number of addresses that is less than a number of addresses required for storage of data corresponding to a predetermined period, and being able to execute a writing operation and a reading operation independently from each other using a clock for writing and a clock for reading, respectively;

a first counter circuit for starting a count of the first clock on receipt of a writing start reference signal indicating a reference timing of starting data writing into the memory, and generating write addresses of the memory, which repeatedly increase or decrease within a predetermined range of addresses of the memory, so that the data corresponding to the predetermined period can be written in the memory over ~~using at least a portion of the addresses of the memory~~ a plurality of times;

a second counter circuit for starting a count of the second clock from a reading start reference signal indicating a reference timing of starting data reading from the memory, and generating read addresses of the memory, which repeatedly increase or decrease within a predetermined range of addresses of the memory, so that the data corresponding to the predetermined period which have been written in the memory can be read from the memory over ~~using at least the portion of the addresses of the memory~~ a plurality of times; and

a delay adjustment circuit operable to adjust a delay time, which delays the writing start reference signal to generate the reading start reference signal.

Claim 5 **(Currently Amended)** A clock conversion apparatus for converting data synchronized with a first clock into data synchronized with a second clock, the clock conversion apparatus comprising:

a memory having a number of addresses that is less than a number of addresses required for storage of data corresponding to a predetermined period, and being able to execute a writing operation and a reading operation independently from each other using a clock for writing and a clock for reading, respectively;

a first counter circuit for starting a count of the first clock on receipt of a writing start reference signal indicating a reference timing of starting data writing into the memory, and generating write addresses of the memory so that the write addresses repeatedly increase or decrease within a predetermined range of addresses of the memory, and a last increase or decrease for every predetermined period is carried out within a range of addresses narrower than the predetermined range of addresses, thereby enabling writing of the data corresponding to the predetermined period into the memory over ~~using at least a portion of the addresses of the memory~~ a plurality of times;

a second counter circuit for starting a count of the second clock from a reading start reference signal indicating a reference timing of starting data reading from the memory, and generating read addresses of the memory so that the read addresses repeatedly increase or decrease within a predetermined range of addresses of the memory, and a last increase or decrease for every predetermined period is carried out within a range of addresses narrower than the predetermined range of addresses, thereby enabling reading of the data corresponding to the predetermined period, which have been written in the memory, over ~~using at least the portion of the addresses of the memory~~ a plurality of times; and

a delay adjustment circuit operable to adjust a delay time, which delays the writing start reference signal to generate the reading start reference signal.

Claim 6 **(Previously Presented)** A clock conversion apparatus as defined in Claim 1, wherein

the data corresponding to the predetermined period are written in the memory using write addresses such that a multiple of a maximum write address value is close to a number of samples of data that are sampled at the first clock within the predetermined period; and

the data are read from the memory using read addresses such that a multiple of a maximum read address value is close to a number of samples of data that are sampled at the second clock.

Claim 7 **(Previously Presented)** A clock conversion apparatus as defined in Claim 1, wherein

the data corresponding to the predetermined period are written in the memory using write addresses such that a multiple of a maximum write address value is close to a number of samples of data that are sampled at the first clock within the predetermined period; and

the data are read from the memory using read addresses having a maximum value equal to the maximum value of the write addresses.

Claim 8 **(Previously Presented)** A clock conversion apparatus as defined in Claim 1, wherein

the predetermined period is one horizontal sync period.

Claim 9 **(Previously Presented)** A clock conversion apparatus as defined in Claim 1, wherein

the first counter circuit comprises:

a write address counter for counting the first clock to create the write addresses; and

a write maximum value limiter for comparing the write address outputted from the write address counter with a settable write maximum value, and resetting the write address counter when the write address becomes equal to the write maximum value.

Claim 10 **(Previously Presented)** A clock conversion apparatus as defined in Claim 1, wherein

the second counter circuit comprises:

a read address counter for counting the second clock to create the read addresses; and

a read maximum value limiter for comparing the read address outputted from the read address counter with a settable read maximum value, and resetting the read address counter when the read address becomes equal to the read maximum value.

Claim 11 **(Currently Amended)** A clock conversion method for converting data synchronized with a first clock into data synchronized with a second clock, the clock conversion method comprising:

generating write addresses of a memory on the basis of the first clock so that data corresponding to a predetermined period are written, over ~~using at least a portion of addresses of the memory~~ a plurality of times, into the memory which has a number of addresses that is less than a number of addresses required for storage of the data corresponding to the predetermined period, and is able to execute a writing operation and a reading operation independently from each other using a clock for writing and a clock for reading, respectively; and

generating read addresses of the memory on the basis of the second clock so that the data corresponding to the predetermined period are read from the memory over ~~using at least the portion of the addresses of the memory~~ a plurality of times.

Claim 12 **(Currently Amended)** A video display apparatus comprising:

a first video processing unit for subjecting a digital video signal to first video processing on the basis of a first clock;

a clock conversion unit for converting the digital video signal which is outputted from the first video processing unit and synchronized with the first clock into a digital video signal synchronized with a second clock;

a second video processing unit for subjecting the digital video signal outputted from the clock conversion unit to second video processing on the basis of the second clock; and

a display device for displaying the digital video signal outputted from the second video processing unit, wherein

the clock conversion unit comprises:

a memory having a capacity less than one horizontal line of the digital video signal outputted from the first video processing unit, and being operable to execute a writing operation and a reading operation independently from each other using a clock for writing and a clock for reading, respectively; and

a memory controller for controlling the memory so that the digital video signal outputted from the first video processing unit are written into the memory over ~~using at least a portion of addresses of the memory~~ a plurality of times for every horizontal line, and the data corresponding to each horizontal line, which are written in the memory, are read from the memory over ~~using at least the portion of the addresses of the memory~~ a plurality of times.

Claim 13 **(Currently Amended)** A video display apparatus as defined in Claim 12, wherein the memory controller comprises:

a first counter circuit for starting a count of the first clock on receipt of a writing start reference signal indicating a reference timing of starting data writing into the memory, and generating write addresses of the memory so that the one horizontal line of data can be written into the memory over ~~using at least the portion of the addresses of the memory~~ a plurality of times; and

a second counter circuit for starting a count of the second clock from a reading start reference signal indicating a reference timing of starting data reading from the memory, and generating read addresses of the memory so that the one horizontal line of data which are written in the memory can be read from the memory over ~~using at least the portion of the addresses of the memory~~ a plurality of times.

Claim 14 **(Currently Amended)** A memory address setting method for a video display apparatus comprising:

a first video processing unit for subjecting a digital video signal to first video processing on the basis of a first clock;

a clock conversion unit for converting the digital video signal which is outputted from the first video processing unit and synchronized with the first clock into a digital video signal synchronized with a second clock;

a second video processing unit for subjecting the digital video signal outputted from the clock conversion unit to second video processing on the basis of the second clock;

a display device for displaying the digital video signal outputted from the second video processing unit, wherein

the clock conversion unit comprises:

a memory having a number of addresses that is less than a number of addresses required for storage of data corresponding to a predetermined period, and being able to execute a writing operation and a reading operation independently from each other using a clock for writing and a clock for reading, respectively;

a first counter circuit for generating write addresses of the memory on the basis of the first clock so that the data corresponding to the predetermined period are written over ~~using at least a portion of the addresses of the memory~~ a plurality of times; and

a second counter circuit for generating read addresses of the memory on the basis of the second clock so that the data corresponding to the predetermined period are read from the memory over ~~using at least the portion of the addresses of the memory~~ a plurality of times,

the memory address setting method comprising:

determining a broadcasting system of the digital video signal inputted to the first video processing unit;

detecting upper limits or lower limits of count values of the first and second counter circuits corresponding to the determined broadcasting system, according to the broadcasting system; and

setting the detected upper limits or lower limits of the count values on the first and second counter circuits.

Claim 15 **(Previously Presented)** A clock conversion apparatus as defined in Claim 2, wherein

the data corresponding to the predetermined period are written in the memory using write addresses such that a multiple of a maximum write address value is close to a number of samples of data that are sampled at the first clock within the predetermined period; and

the data are read from the memory using read addresses such that a multiple of a maximum read address value is close to a number of samples of data that are sampled at the second clock.

Claim 16 **(Previously Presented)** A clock conversion apparatus as defined in Claim 3, wherein

the data corresponding to the predetermined period are written in the memory using write addresses such that a multiple of a maximum write address value is close to a number of samples of data that are sampled at the first clock within the predetermined period; and

the data are read from the memory using read addresses such that a multiple of a maximum read address value is close to a number of samples of data that are sampled at the second clock.

Claim 17 **(Previously Presented)** A clock conversion apparatus as defined in Claim 4, wherein

the data corresponding to the predetermined period are written in the memory using write addresses such that a multiple of a maximum write address value is close to a number of samples of data that are sampled at the first clock within the predetermined period; and

the data are read from the memory using read addresses such that a multiple of a maximum read address value is close to a number of samples of data that are sampled at the second clock.

Claim 18 **(Previously Presented)** A clock conversion apparatus as defined in Claim 5, wherein

the data corresponding to the predetermined period are written in the memory using write addresses such that a multiple of a maximum write address value is close to a number of samples of data that are sampled at the first clock within the predetermined period; and

the data are read from the memory using read addresses such that a multiple of a maximum read address value is close to a number of samples of data that are sampled at the second clock.

Claim 19 **(Previously Presented)** A clock conversion apparatus as defined in Claim 2, wherein

the data corresponding to the predetermined period are written in the memory using write addresses such that a multiple of a maximum write address value is close to a number of samples of data that are sampled at the first clock within the predetermined period; and

the data are read from the memory using read addresses having a maximum value equal to the maximum value of the write addresses.

Claim 20 **(Previously Presented)** A clock conversion apparatus as defined in Claim 3, wherein

the data corresponding to the predetermined period are written in the memory using write addresses such that a multiple of a maximum write address value is close to a number of samples of data that are sampled at the first clock within the predetermined period; and

the data are read from the memory using read addresses having a maximum value equal to the maximum value of the write addresses.

Claim 21 **(Previously Presented)** A clock conversion apparatus as defined in Claim 4, wherein

the data corresponding to the predetermined period are written in the memory using write addresses such that a multiple of a maximum write address value is close to a number of samples of data that are sampled at the first clock within the predetermined period; and

the data are read from the memory using read addresses having a maximum value equal to the maximum value of the write addresses.

Claim 22 **(Previously Presented)** A clock conversion apparatus as defined in Claim 5, wherein

the data corresponding to the predetermined period are written in the memory using write addresses such that a multiple of a maximum write address value is close to a number of samples of data that are sampled at the first clock within the predetermined period; and

the data are read from the memory using read addresses having a maximum value equal to the maximum value of the write addresses.

Claim 23 **(Previously Presented)** A clock conversion apparatus as defined in Claim 2, wherein

the predetermined period is one horizontal sync period.

Claim 24 **(Previously Presented)** A clock conversion apparatus as defined in Claim 3, wherein the predetermined period is one horizontal sync period.

Claim 25 **(Previously Presented)** A clock conversion apparatus as defined in Claim 4, wherein the predetermined period is one horizontal sync period.

Claim 26 **(Previously Presented)** A clock conversion apparatus as defined in Claim 5, wherein the predetermined period is one horizontal sync period.

Claim 27 **(Previously Presented)** A clock conversion apparatus as defined in Claim 2, wherein the first counter circuit comprises:

a write address counter for counting the first clock to create the write addresses; and

a write maximum value limiter for comparing the write address outputted from the write address counter with a settable write maximum value, and resetting the write address counter when the write address becomes equal to the write maximum value.

Claim 28 **(Previously Presented)** A clock conversion apparatus as defined in Claim 3, wherein the first counter circuit comprises:

a write address counter for counting the first clock to create the write addresses; and

a write maximum value limiter for comparing the write address outputted from the write address counter with a settable write maximum value, and resetting the write address counter when the write address becomes equal to the write maximum value.

Claim 29 **(Previously Presented)** A clock conversion apparatus as defined in Claim 4, wherein the first counter circuit comprises:

a write address counter for counting the first clock to create the write addresses; and

a write maximum value limiter for comparing the write address outputted from the write address counter with a settable write maximum value, and resetting the write address counter when the write address becomes equal to the write maximum value.

Claim 30 **(Previously Presented)** A clock conversion apparatus as defined in Claim 5, wherein

the first counter circuit comprises:

a write address counter for counting the first clock to create the write addresses; and

a write maximum value limiter for comparing the write address outputted from the write address counter with a settable write maximum value, and resetting the write address counter when the write address becomes equal to the write maximum value.

Claim 31 **(Previously Presented)** A clock conversion apparatus as defined in Claim 2, wherein

the second counter circuit comprises:

a read address counter for counting the second clock to create the read addresses; and

a read maximum value limiter for comparing the read address outputted from the read address counter with a settable read maximum value, and resetting the read address counter when the read address becomes equal to the read maximum value.

Claim 32 **(Previously Presented)** A clock conversion apparatus as defined in Claim 3, wherein

the second counter circuit comprises:

a read address counter for counting the second clock to create the read addresses; and

a read maximum value limiter for comparing the read address outputted from the read address counter with a settable read maximum value, and resetting the read address counter when the read address becomes equal to the read maximum value.

Claim 33 **(Previously Presented)** A clock conversion apparatus as defined in Claim 4, wherein

the second counter circuit comprises:

a read address counter for counting the second clock to create the read addresses; and

a read maximum value limiter for comparing the read address outputted from the read address counter with a settable read maximum value, and resetting the read address counter when the read address becomes equal to the read maximum value.

Claim 34 **(Previously Presented)** A clock conversion apparatus as defined in Claim 5, wherein

the second counter circuit comprises:

a read address counter for counting the second clock to create the read addresses; and

a read maximum value limiter for comparing the read address outputted from the read address counter with a settable read maximum value, and resetting the read address counter when the read address becomes equal to the read maximum value.